09/540,471

Dopant Diffusion Barrier Layer For Use In III-V Structures

Cross-Reference To Related Applications

This present application claims priority of Provisional Application Serial No. 60/175,010 (~~Attorney Docket Number: Y. Akulova 1-4-2~~). The present application is also related to U.S. Patent Application Serial No. (~~Attorney Docket Numbers Akulova 2-14-11-5-7-8~~ and ~~Geva 5-1-3-20~~) 09/539,882 and 60/175009 filed on even date herewith and assigned to the assignee of the present invention. The disclosures of the above captioned patent applications are specifically incorporated herein by reference.

PS 10/18/04

Field of the Invention

The present invention relates to a dual layer dopant diffusion barrier for use in III-V semiconductor structures.

Background of the Invention

One typical structure employed in optoelectronic devices is the p-i-n (PIN) structure. In a typical PIN structure, an intrinsic layer is disposed between a p-type layer and a n-type layer, forming a heterostructure device. The intrinsic layer has a larger index of refraction than the p and n layers resulting in a natural waveguide. Furthermore, the energy band discontinuities in the conduction and valence bands in the PIN structure facilitate carrier confinement within the active layer. In short, the PIN structure is well suited for a variety of emitting and detecting optoelectronic device applications.

One material that is often used in optoelectronics devices is indium phosphide (InP). In a PIN structure employing InP, a p-type layer is often fabricated by introducing zinc as a dopant. While zinc is a suitable dopant for forming p-type layer, zinc can readily diffuse due to the higher temperature achieved during the growth of InP. Diffusion into the active (intrinsic layer in a PINstructure) layer can occur resulting in the undesired doping of the active layer. This can have deleterious effects. For example, in a